REMARKS

Reconsideration of this application is respectfully requested in view of the foregoing amendment and the following remarks.

By the foregoing amendment, new claims 18-20 have been added. Thus, claims 1-20 are currently pending in the application and are subject to examination.

In the Office Action mailed February 12, 2004, the Examiner rejected claims 1-2, 11 and 16-17 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,818,433 to Sherburne in view of U.S. Patent No. 4,755,810 to Knierim. The Examiner rejected claims 3, 5-7, and 8-10 under 35 U.S.C. § 103(a) as being unpatentable over Sherburne in view of Knierim and further in view of U.S. Patent No. 6,175,388 to Knox, et al. Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Sherburne in view of Knierim and further in view of U.S. Patent No. 5,883,675 to Herz, et al. Claim 12 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Knox, et al. in view of U.S. Patent No. 6,233,658 to Tamura. The Examiner rejected claim 13 under 35 U.S.C. § 103(a) as being unpatentable over Knox, et al. in view of Tamura and further in view of U.S. Patent No. 6,300,964 to Intihar. Claim 14 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Knox, et al. in view of Tamura and further in view of U.S. Patent No. 5,227,863 to Bilbrey, et al. The Examiner rejected claim 15 under 35 U.S.C. § 103(a) as being unpatentable over Knox, et al. in view of Tamura and further in view of U.S. Patent No. 5,673,087 to Choi, et al. The Applicants hereby traverse the rejections, as follows.

With respect to claim 1, in response to Applicants' arguments made in the Amendment of November 20, 2003, the Examiner indicates that claim 1 "does not

mention that the width is adjusted . . . [and that] Sherburne teaches changing the size of the memory depending on the size of the image data and the overlay data." The Examiner also states that "[i]t was well known to store data in memory at address locations to better organize the data." See Office Action, at page 2. The Examiner further indicates that Sherburne teaches each and every limitation of claim 1, with the exception of "a refresh circuit controlling refreshing of said storage circuit," and cites Knierim for curing this deficiency of Sherburne. See Office Action, at page 5.

Applicants submit, however, that neither Sherburne nor Knierim, nor the combination thereof, discloses or suggests each and every limitation of claim 1. Sherburne only discloses an apparatus and methods for the organization, storage and playback of graphics data for display purposes. The image data and overlay data (and/or other graphics data) are organized and stored in the graphics memory in an interleaved fashion, so that only one type of graphics data is stored at any one memory address and so that preferably full memory capacity is utilized for the area of graphics memory employed. Neither Sherburne nor Knierim, nor the combination thereof teaches or suggests at least the limitation of an "area adjustment circuit which sets up an additional area adjacent to an area in which the image data are actually stored in a memory space of said storage circuit and storing therein additional data other than the image data, which adjusts the address generated by said address generation circuit," as required by independent claim 1.

For at least this reason, Applicants submit that claim 1, is allowable over the cited prior art. As claim 1, is allowable, Applicants submit that claims 2-11, as well as

newly added claim 18, each of which depend from allowable claim 1, are likewise allowable over the cited prior art.

Similarly to as discussed above with regard to claim 1, Applicants submit that claim 16 is allowable over the cited prior art at least because the cited prior art does not disclose or suggest the limitation of an area adjustment circuit which sets up an additional area adjacent to an area in which the image data are actually stored in a memory space of said storage circuit and storing therein additional data other than the image data, which adjusts the address generated by said address generation circuit.

As claim 16 is allowable, Applicants submit that newly added claim 19, depending from allowable claim 16, is likewise allowable over the cited prior art.

With regard to claim 17, Applicants submit that claim 17 is allowable over the cited prior art at least because the cited prior art does not disclose or suggest the limitation of setting up an additional address space of a width same as the address space for a range of an additional area which is adjacent to the image area and in which data other than the image data is written, with information supplied to a memory space of said storage circuit as a parameter, as required by claim 17.

As claim 17 is allowable, Applicants submit that newly added claim 20, depending from allowable claim 17, is likewise allowable over the cited prior art.

Regarding claim 12, the Examiner notes that Knox, et al. discloses substantially all of the elements of the claimed invention with the exception of showing "writing the image data . . . according to a second write control signal and writing the additional data with a first write control signal and reading out the additional data . . . and the image data stored in the image area . . . in response to a first read control signal." See Office

Action, at page 3. The Examiner cites Tamura for curing the deficiencies that exist in Knox, et al.

Applicants submit, however, that neither Knox, et al. nor Tamura, nor the combination thereof, discloses or suggests each and every limitation of claim 12. It is submitted that Knox, et al. discloses a method and apparatus for generating On-Screen Display ("OSD") messages. The Knox, et al. OSD data is disclosed as "pixel data," and the output of the OSD unit is "streams or sequences of digital words representing respective luminance and chrominance components." See Knox, et al., Column 3 Line 42 and Column 4, Lines 31-33. Nothing in Knox, et al. teaches or suggests at least the combination of "setting up . . . a range of an additional area which is adjacent to the image area and in which data other than the image data is written" and "writing the additional data . . . into the additional area . . . wherein the additional data are written in with an address of the additional area," as claimed in claim 12.

In addition, Applicants respectfully submit that nothing in Tamura cures the deficiencies that, according to the Examiner, exist in Knox, et al. Tamura teaches a memory control system in which serial input image data are sequentially written into N image memories in rotation. Then, image data is concurrently read from each of the N image memories depending on a desired read position to produce N image data in parallel. Tamura only teaches sequentially writing image data into N memories. See, e.g., Tamura, Column 1, Lines 36-51. Additionally, Tamura fails to teach or suggest reading image and non-image data "in response to a first read control signal," as also required by claim 12.

For at least these reasons, Applicants submit that claim 12, is allowable over the cited prior art. As claim 12, is allowable, Applicants submit that claims 13-15, each of which depend from allowable claim 12, are likewise allowable over the cited prior art.

With regard to each of the rejections under §103 in the Office Action, it is also respectfully submitted that the Examiner has not yet set forth a *prima facie* case of obviousness. The PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 U.S.P.Q.2nd 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 U.S.P.Q. 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002).

With respect to claim 1, for example, the Examiner merely states that it "would have been obvious to one of ordinary skill in the art . . . to use the refresh circuit of Knierim with the system of Sherburne because this would have kept the screen from flickering. See, e.g., Office Action at page 5. There is nothing in the references,

however, to suggest this modification. Therefore, this is an insufficient showing of motivation.

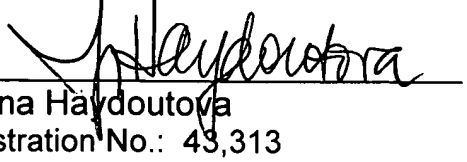
For all of the above reasons, it is respectfully submitted that the claims now pending patentability distinguish the present invention from the cited references. Accordingly, reconsideration and withdrawal of the outstanding rejections and an issuance of a Notice of Allowance are earnestly solicited.

Should the Examiner determine that any further action is necessary to place this application into better form, the Examiner is encouraged to telephone the undersigned representative at the number listed below.

In the event this paper is not considered to be timely filed, Applicants hereby petition for an appropriate extension of time. The fee for this extension may be charged to our Deposit Account No. 01-2300, referring to client-matter number 024354-00001. The Commissioner is hereby authorized to charge any fee deficiency or credit any overpayment associated with this communication to Deposit Account No. 01-2300, referring to client-matter number 024354-00001.

Respectfully submitted,

ARENT FOX PLLC



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